MICROCHIP

AN536

Basic Serial EEPROM Operation

BASIC SERIAL EEPROM OPERATION

Looking for the optimum non-volatile memory product for your system that requires a small footprint, byte level flexibility, low power, and is highly cost effective? Serial EEPROM technology is one of the non-volatile memory technologies that has emerged as a leading embedded control solution. Unfortunately, most system designers are not aware of the serial EEPROM benefits. Also, the supporting documentation in databooks is most often not adequate due to incomplete or ambiguous information. As a result, the system designer often selects a non-volatile solution that does not meet his requirements, or, the designer must face a more complicated design-in with a serial EEPROM.

This article addresses two issues that exist today for designers considering serial EEPROM products:

First, to provide awareness of the application benefits.

Secondly, to provide a primer on the operating principles and instructions. These items are often buried in databook text or not adequately addressed. Also included are common default conditions to significantly reduce the system designer's learning curve.

CONTENTS

SERIAL EEPROM APPLICATIONS

Serial EEPROMS are ideal non-volatile cost effective memory solutions in applications that require:

- Small footprint and board space as in cellular phone applications
- BYTE level ERASE, WRITE, and READ of data as in a TV tuner
- Low voltage and current for handheld battery applications as in a keyless entry transmitter
- Multiple non-volatile functions in the same application such as a VCR
- Low availability of microcontroller I/O lines

The common applications for Serial EEPROMS are shown below:

Market	Common Applications
Consumer	TV tuners, VCRs, CD players, cameras, radios, and remote controls
Automotive	Airbags, anti-lock brakes, odometers, radios, and keyless entry
Office Automation	Printers, copiers, PCs, and portable PCs
Telecom	Cellular, cordless and full feature phones, faxes, modems, pagers, and satellite receivers
Industrial	Bar code readers, point-of-sale terminals, smart cards, lock boxes, garage door openers, and test measurement equipment

The typical functions that serial EEPROMs are utilized for are:

- Memory storage of channel selectors or analog controls (volume, tone, etc.) in consumer electronics products
- Power down storage and retrieval of events such as fault detection or error diagnostics in automotive products
- Electronic real time event or maintenance logs such as page counting in office automation products. Also, configuration or DIP switch storage in office automation products
- Last number redial storage and speed dial number storage in telecom products
- User in-circuit reprogrammable look up tables such as bar code readers, point-of-sale terminals, environmental controls and other industrial products

Other application examples include:

- Data storage from a learn function as in a remote control transmitter
- ID number storage for security or remote access for electronic keys and entry databases
- Reprogrammable calibration data for test equipment or analog interface products

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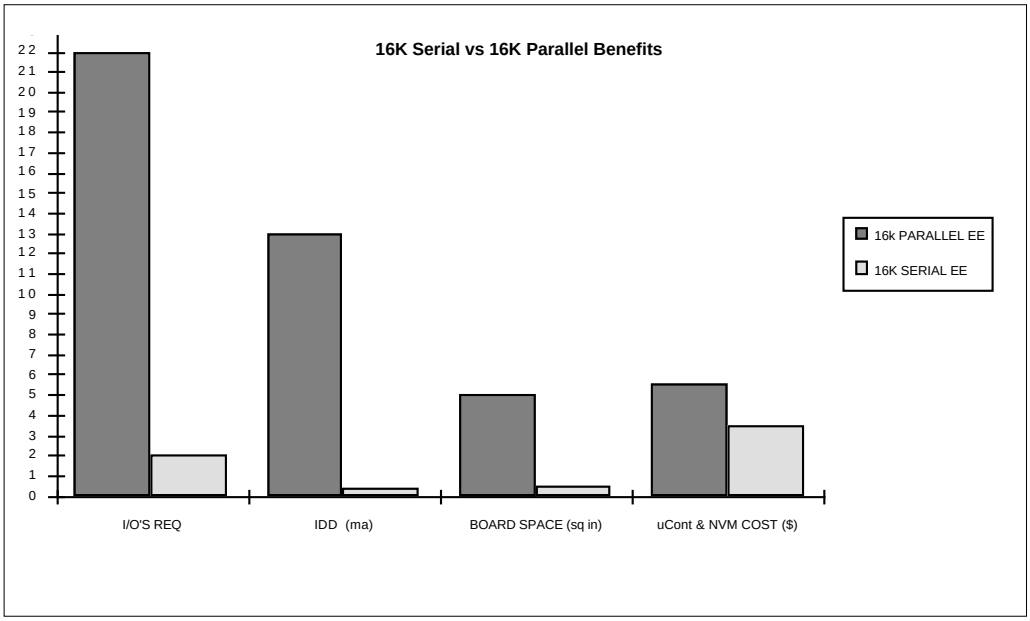
As a result of density and architectural evolution, Serial EEPROMs offer significant benefits in some applications that previously could only utilize Parallel EEPROM products. The diagram below illustrates the footprint and board space differences.



The Serial EEPROM requires only 10% of the board space that a Parallel EEPROM requires. Also, the Serial EEPROM requires fewer I/O lines from the microcontroller which significantly reduces the overall system cost and board space.

A very fast READ speed is the only significant limitation of a Serial EEPROM for a decision between a serial and a Parallel EEPROM. It is very interesting to note that the Serial EEPROM READ speed is restricted more by the protocol than the process technology. The 2-wire I²C (Inter-Integrated Circuit) products must add large internal delays to slow down the part to meet the 100KHz protocol requirements, which will be reviewed later. Characterization of 3-wire bus Serial EEPROMs have indicated clock frequencies in excess of 6MHz.

OVERVIEW OF THE PRIMARY PROTOCOL BENEFITS

After a designer decides to use a serial EEPROM solution, the next step is to select one of the two primary serial EEPROM protocols. Unfortunately, most system designers select the type of serial EEPROM (2- or 3-wire) that they are most familiar with, regardless of the benefits associated with each type.

The benefits of each protocol are shown below:

3-Wire Bus Serial EEPROMS	2-Wire Bus Serial EEPROMS
Single V_{DD} supply of <2V to 5.5V	Single V_{DD} supply of <2V to 5.5V
Very low current consumption	Very low current consumption
Reduced overall component cost	Reduced overall component cost
Four pins (other than V_{CC} & GND) are required or operation	Two pins (other than V_{CC} & GND) are required for operation
x16 bit and x8 bit data widths	x8 data bit width
Software WRITE Protection	Hardware WRITE Protection
Edge triggered clocks and signals	Level triggered clocks and signals and input glitch filters for high noise immunity
2MHz+ operation	I^2C standard 100KHz and 400KHz protocols with a 1MHz option
Ready/Busy data polling	Page WRITE capability to 16 bytes
Security options available	Software and hardware compatible from 2K to 16K densities
Less complex protocol	

A 2- wire product is utilized in applications that require an I^2C bus, noise immunity, limited microcontroller I/O pin availability, or a WRITE buffer for multiple bytes to be stored with one instruction. A 3-wire product is utilized in applications that have limited protocol requirements, an SPI protocol, higher clock frequency requirements, or x16 data width applications.

The next two sections describe the basic operation and Microchip's default conditions for the 3-wire and 2-wire Serial EEPROMs to allow the system designer to utilize the benefits of Serial EEPROMs.

3-WIRE BUS OPERATION PRIMER

Many serial EEPROM data sheets are written in a conventional memory data sheet format which emphasizes the features of the part more than the basic operating principles. The operating principles are unfortunately either vaguely embedded in the data sheet text or not included. Serial EEPROMs are not conventional memories due to the Serial communication protocols involved. This section is a PRIMER for the data sheet to familiarize the system designer with the basic principles of the 3-wire bus operation.

Basic Principles

Common device nomenclature is 93XXXX.

The 93XX06 is a 256 bit product.

The 93XX46 is a 1K bit product.

The 93XX56 is a 2K bit product.

The 93XX66 is a 4K bit product.

Four pins are required:

CS (Chip Select)	DI (data in)
CLK (Clock)	DO (data out)

All 93XXXX parts are hardware compatible for these four pins. However, there may be compatibility issues for the other pins.

Even though there is hardware compatibility on the four pins, there can be differences from a software standpoint. Subtle differences between each manufacturer's products, referred to as default conditions, can prevent plug compatibility. These issues are addressed later in the attached 3-Wire Timing Diagram. There is no industry standardized upgrade path for density migration. Please review density upgrades for Microchip's products on a case-by-case basis.

Data is available in x8 or x16 organizations. This selection is determined either by the ORG pin or by purchasing a standard x16 organization.

Units will power-up in a EWDS (ERASE/WRITE Disable State). All ERASE and WRITE functions are disabled until the EWEN (ERASE/WRITE Enable) instruction is performed. This is to prevent accidental data corruption.

An Auto-ERASE (logical "1") cycle is performed during each WRITE Cycle.

The 7 instructions are shown in the attached instruction set table. These instructions are for Microchip's 93LCXX family products.

After an instruction is loaded, the CLK and DI pins are in a DON'T CARE state until the next START bit.

The following is required for each instruction set (all input bits are triggered by the positive clock edges):

Start Bit	The first Data-in high signal clocked in after CS is high.
Opcode	Two Bits to identify the instruction
Address	Refer to the Instruction Set table for the number of bits required.
Data	Separate data-in and data-out pins. However, these two pins may be tied together for true 3-wire operation. Please refer to the attached 3-wire Bus READ timing diagram example.

READ, WRITE, and ERASE

The attached 93LC66 timing diagrams illustrate the key concepts and timing parameters for each of these operations. Please refer to the instruction set tables and the AC parameters in the databook for supplemental information.

ERASE ALL (ERAL)

An ERASE ALL (ERAL) operation is identified by a “00” opcode. The ERAL instruction requires the next two bits to be clocked in as “10” in the address block of the instruction set. All bits in the array will be set to a logic “1” state by one command in typically less than 10ms.

WRITE ALL (WRAL)

A WRITE ALL (WRAL) operation is also identified by a “00” opcode. The WRAL requires the next two bits to be clocked in as “01” in the address block of the instruction set. The data-in block will contain the data for a SINGLE BYTE which is to be repeated throughout the entire array. For example, if a 4F5A is loaded in the 16 data-in bits of the instruction set, a 4F5A will be written into every word in the array.

EWEN and EWDS

As stated before, all units will power up in to an ERASE/WRITE DISABLE (EWDS) state to prevent data corruption. All future ERASE/WRITE operations must execute an ERASE/WRITE ENABLE (EWEN) opcode until the next power down is detected or until other EWDS opcodes are executed. Please refer to the instruction set table.

INSTRUCTION SET FOR 93LC46: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{\text{BSY}}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

INSTRUCTION SET FOR 93LC46: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{\text{BSY}}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

INSTRUCTION SET FOR 93LC56: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93LC56: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

INSTRUCTION SET FOR 93LC66: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 - A0	—	D15 - D0	27
EWEN	1	00	11XXXXXX	—	High-Z	11
ERASE	1	11	A7 - A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	10XXXXXX	—	(RDY/$\overline{\text{BSY}}$)	11
WRITE	1	01	A7 - A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	01XXXXXX	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
EWDS	1	00	00XXXXXX	—	High-Z	11

INSTRUCTION SET FOR 93LC66: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 - A0	—	D7 - D0	20
EWEN	1	00	11XXXXXXX	—	High-Z	12
ERASE	1	11	A8 - A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	10XXXXXXX	—	(RDY/$\overline{\text{BSY}}$)	12
WRITE	1	01	A8 - A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	01XXXXXXX	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
EWDS	1	00	00XXXXXXX	—	High-Z	12

2-WIRE BUS OPERATION PRIMER

As indicated in the 3-wire bus section, many serial EEPROM data sheets are written in a conventional memory data sheet format which emphasizes the features of the part more than the basic operating principles. The operating principles are, unfortunately, either vaguely embedded in the data sheet text or not included. This section is a PRIMER for the data sheet to familiarize the system designer with the basic 2-wire serial EEPROM operation principles.

Basic Principles

The common device nomenclature is 24XXXX and 85XXXX.

Only the SCL and SDA pins are essential for bus operation. The other pins are supplementary:

SCL (Serial clock)

SDA (Serial Data)

WP (Active High WRITE Protection)

A0, V A1, and A2 (Chip or block select)

SDA's open-drain requires a pull-up resistor to V_{DD}.

The data is organized as x8.

Signals are level triggered, not edge triggered. Also, there are filters on the inputs that will filter noise glitches <100ns wide.

An Auto-ERASE (logical "1") cycle is performed during each WRITE cycle.

The I^2C protocol utilizes master/slave bi-directional communication. A device that sends data onto the bus is defined as the transmitter, and a device that is receiving data is the receiver. Both the master and the slave can operate as the transmitter or receiver. The bus must be controlled by a master device (most often a microcontroller), which generates the serial clock (SCL), controls the bus direction, and generates the START and the STOP conditions.

The serial EEPROM is the slave. The serial EEPROM will be the bus transmitter during READ operations and when the serial EEPROM must acknowledge data transmitted by the master.

START and STOP bits control the bus activity. Operations must begin with a START bit and end with a STOP bit.

A START bit is when SDA transitions LOW while SCL is HIGH while observing the START set-up and hold time specifications.

A STOP bit is when SDA transitions HIGH while SCL is HIGH while observing the STOP set-up and hold time specifications.

Data is recognized as valid while SCL is high. The data on SDA must observe data in set-up and hold specifications before and after SCL is pulsed. There is only one bit of data for each SCL pulse.

Control Byte Requirements

After a START bit, each command begins with an 8 bit control byte sent by the master. This control byte has the following three primary functions before the data and/or word address information is loaded for all commands:

Identify the serial EEPROM as the slave addressed on the bus.

Select the specific serial EEPROM or the internal memory block on the bus. There may be up to 8 serial EEPROMs on the bus)

Select the READ or WRITE function for the next command transmitted by the master.

The diagram of a control byte (not including the START bit) is shown below:

1	0	1	0	A2	A1	A0	X
I^2C Slave Address				Chip or Block Select			Read or W rite bit

Control Bits 1-4 are the Slave Address Bits (Must be 1010 for Memory)

Since there is not a chip select pin, the part is selected by a four bit code in the control byte to identify the type of product. The four bit code was established by Philips for the I^2C protocol. A 1010 code identifies the slave device as a Serial EEPROM. The Serial EEPROM will remain in stand-by until the 1010 code is transmitted on the bus. Other non Serial EEPROM slave devices will not respond to the 1010 code on the bus.

Control Bits 5-7 are the 1 of 8 Chip or Block Address Select Bits

The next three control bits are utilized for the chip selection or internal block selection. The standard I^2C protocol was developed to allow up to 16K bits of memory to be selected. This could be accomplished by accessing a combination of devices or blocks within a device, as shown in the table on the following page:

Device	K bits Density	Internal Blocks	A0	A1	A2	Bus Access Devices
24LC01B, 24C01,85C72	1	1	H or L	H or L	H or L	Up to 8 devices
24LC02B, 24C02,85C82	2	1	H or L	H or L	H or L	Up to 8 devices
24LC04B, 24C04,85C92	4	2	X	H or L	H or L	Up to 4 devices
24LC08B	8	4	X	X	H or L	Up to 2 devices
24LC16B	16	8	X	X	X	Only 1 device

X= NOT USED. This pin must be tied to VSS or VDD. It is not recommended to FLOAT these pins since there may be test modes accessed to these pins via a high voltage signal.

These three bits for this select must match the hardware conditions (IF ANY ARE USED) of the external A0, A1, and A2 pins or the internal block selects.

With this selection scheme, devices from 2K to 16K are software compatible. For example, four 2K devices or one 8K device could be connected to the bus with the same software.

The A0, A1, and A2 signals are the same for the 1K and 2K products. The A7 bit for the 1K product is a DON'T CARE.

The A0, A1, and A2 pins are not commonly used today in the industry with the advent of the density evolution up to the I^2C protocol limit of 16K bits.

Control Bit 8 Operation Code

If this bit is a "1" then the operation will be a READ

If this bit is a "0" then the operation will be a WRITE

After the control byte acknowledge bit is generated by the serial EEPROM, the master will send the appropriate word address and data information.

Acknowledge Requirements

The serial EEPROM must generate an acknowledge bit after receiving each byte segment in a command. The serial EEPROM will generate the acknowledge bit automatically after the master has transmitted all of the data for the segment.

To acknowledge the master, the serial EEPROM must pull the SDA line LOW during the entire HIGH period of the next clock generated by the master. During the READ operations, the master must acknowledge each data byte or the serial EEPROM will abort the READ operation and return to a stand-by mode waiting for the next START bit.

The attached 24LC16 timing diagrams illustrate the READ and WRITE operations.

MICROCHIP 2-WIRE DEFAULT CONDITIONS

As stated before, data sheets do not provide adequate information on basic operation. This lack of information forces each reader of the databook to make interpretations about the operating conditions. These readers have included other semiconductor circuit designers, which unfortunately leads to subtle compatibility problems. The part is designed to operate to the default of the circuit designer's interpretation. This next section details Microchip's default conditions to help the system engineer minimize "Trial and Error" prototyping and to increase the awareness of these default conditions.

Also, to improve corporate-wide compatibility, Microchip is standardizing their circuits on various product versions. Unless indicated otherwise, all references to default conditions are for the 24LCXX products, not the 24CXXXX products.

Power Up

READ, WRITE, and ERASE operations are valid 5 uS after VDD has ramped to the specified operating range.

PAGE WRITE by Product for Multiple BYTE WRITE Operation

The 24C01 and 24C02 have a 2 byte buffer.

The 24C04 has an 8 byte buffer.

The 24LC01 and 24LC02 have an 8 byte page.

The 24LC04, 24LC08, and 24LC16 have a 16 byte page.

The buffer will load bytes identically as the page loads bytes. The difference in the two modes is that the buffer will execute a WRITE of one byte per WRITE cycle in sequence. The page mode will execute all bytes loaded in one WRITE cycle in parallel.

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There are pages within blocks. For a 16 byte page product, the most significant 4 bits of the word address point to the page address and the least significant 4 bits point to the byte address within a page. For an 8 byte page product, the most significant 5 bits of the word address point to the page address and the least significant 3 bits point to the byte address within a page.

The number of bytes loaded in to the page is from one byte up to the page size. For example, three bytes can be loaded into the 16 byte page of the 24LC16. If during the loading of the fourth byte a STOP bit is received, the page will WRITE three bytes. The fourth byte will not be written since loading the fourth byte was not complete.

NOTE: New versions released in March 1993 will default to ABORTING the entire operation if a STOP bit is received in the middle of a byte while loading a page.

If more than 16 bytes are loaded in the page of a 16 byte page product, then the 17th byte will override the data loaded into the original first byte (the page data will wrap around WITHIN a page). Therefore, the system designer must take precautions to not WRITE over a page boundary during a multiple byte WRITE operation.

Bytes not changed in the page will NOT result in data corruption in the array. For example, If two bytes are loaded in to the 24LC16 page with the least significant word address bits of 0000 and then a STOP bit is transmitted. Bytes 1 and 2 in the array will have the data changed to the new page contents. Bytes 3 through 16 WILL NOT change.

The WRITE operation will not be executed until a STOP bit is transmitted.

At this point, the serial EEPROM is free from the bus since the actual WRITE function is self-timed. Therefore, the microcontroller interfacing to the serial EEPROM may perform other functions not associated to communication with the serial EEPROM during the self-timed WRITE operations.

Once the part is in the auto-ERASE mode, it will complete the ERASE/WRITE operation unless power is removed. STOP and START bits will be ignored.

READ

Once the Serial EEPROM is in a RANDOM READ operation, it can be placed into the sequential READ operation. If the master issues an acknowledge bit instead of a STOP bit, the Serial EEPROM will READ the next sequential 8 bits. The Serial will wait for the next bit command from the master. The sequential READ will continue as long as the master issues an acknowledge bit on the next clock cycle after the last bit is READ. The READ will continue from block to block and will wrap around if the last bit in the array is addressed. Again, this will continue until the master issues a STOP bit instead of an acknowledge bit.

While reading zeroes the master cannot pull SDA high to generate a STOP bit, since the serial EEPROM SDA pin is outputting a low. To recover from a fault during a READ, repeat 9 clocks with data floating high. Therefore, the acknowledge bit will not occur and the part will reset and return to stand-by.

A START bit during an operation will cease the current operation and begin the next operation.

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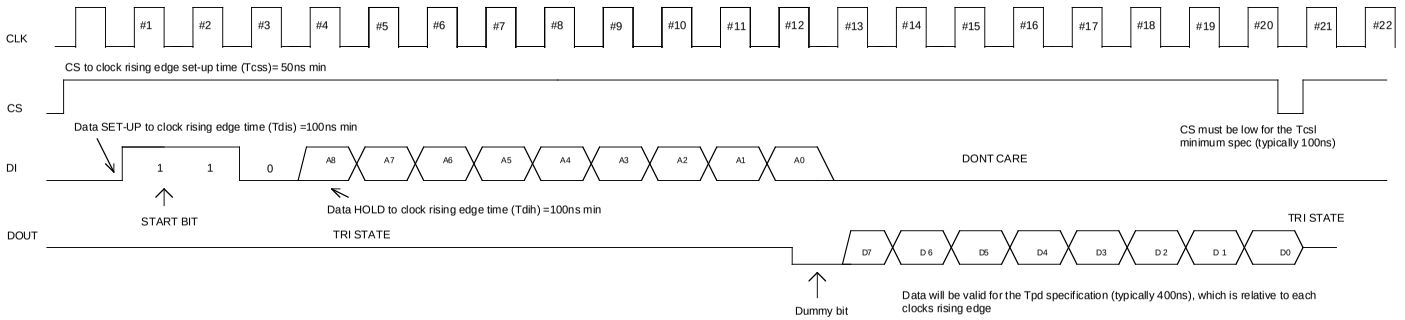
3 WIRE BUS EXAMPLE

MICROCHIP 93LC66 READ CYCLE TIMING DIAGRAM



NOTE: THIS EXAMPLE IS FOR X8 OPERATION OF MICROCHIP'S 93LC66.
INSTRUCTION LENGHTS MAY VARY WITH ARRAY SIZE AND DATA WIDTHS

Data must conform to specified set-up and hold times (Tdis and Tdih) relative to the RISING clock edge. Each parameter is typically 100ns.

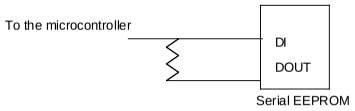
A Read operation is identified by the "1 0 " op-code following the start bit.

Next, the address location bits are loaded.

Then the address contents are clocked out on the rising clock pulse edge. Data will become valid on the DOUT pin per the specified Tpd time (typically 400ns) relative to the rising edge of the clock on the DOUT pin. Note, the first bit output will be a "dummy bit" with a logical zero state. This event is triggered by the clock rising edge of the last address bit for a duration of one clock pulse.

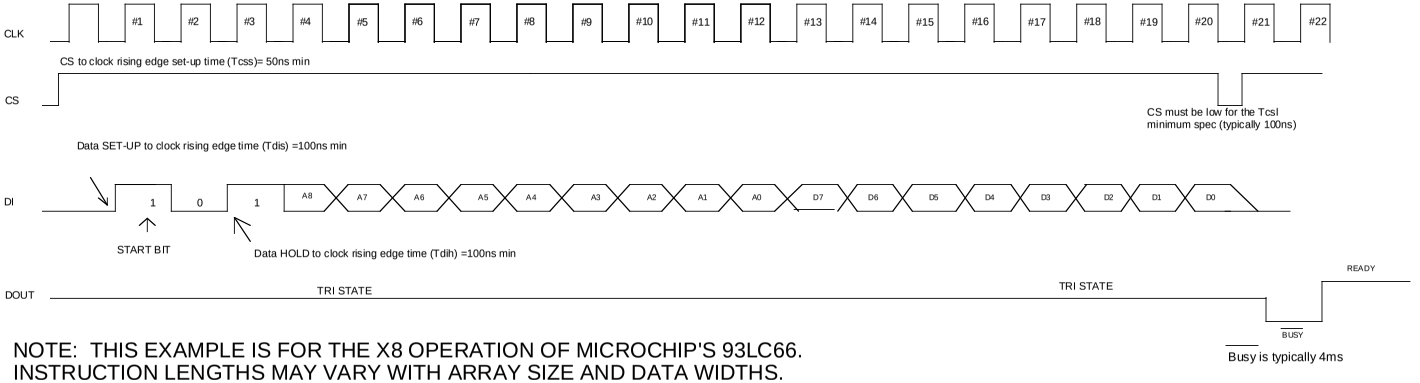
If the data from the current address is complete and the clock pulses continue, the data from the next address will be READ automatically as long as CS remains high. This is the SEQUENTIAL READ FUNCTION. READ operations will continue while clock pulses continue or until CS is brought low.

It is possible to tie the DOUT pin and the DI pin together to save on I/O requirements from the microcontroller. Caution must be exercised to avoid bus contention for an A0 high condition, because of the dummy bit. It recommended that a resistor between the microcontroller port connected to the DI pin and DOUT pin be added for isolation. This example is shown below:



3 WIRE BUS EXAMPLE

MICROCHIP'S 93LC66 WRITE CYCLE TIMING DIAGRAM



NOTE: THIS EXAMPLE IS FOR THE X8 OPERATION OF MICROCHIP'S 93LC66.
INSTRUCTION LENGTHS MAY VARY WITH ARRAY SIZE AND DATA WIDTHS.

Data must conform to specific set-up and hold times (Tdis and Tdih) relative to the clock edge. Each parameter is typically 100ns.

A WRITE operation is identified by a the "0 1 " op code following the start bit

Next, the address location bits are loaded on the DI pin.

Then, the data bits to be written are loaded on the DI pin.

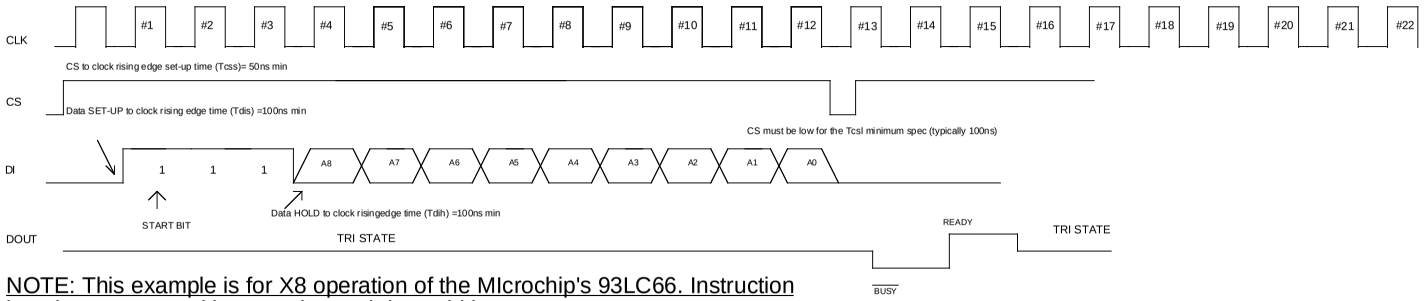
CS must be brought low after the last DI bit is loaded. When CS is brought low for the Tcsl period, a self timed WRITE is executed. If too many bits are loaded during ERASE and WRITE instructions prior to CS being brought low at the end of an instruction set, then the extra bits will be ignored. Only the first bits loaded will be executed.

The DOUT pins only function during a WRITE is to indicate the status of the write with the READY/$\overline{\text{BUSY}}$ function. While DOUT is low, the Serial EEPROM is indicating that programming is not complete (the part is BUSY). When DOUT is high,the Serial EEPROM is indicating that programming is complete and it is READY for another instruction. Note CS must be brought high after completing the Tcsl time is complete to initiate the READY/ BUSY function. Microchip's 93LCXX products can be polled multiple times for the same cycle.

Up through clock pulse 20, data for the instruction is being LOADED. When the CS goes low, the instruction is being EXECUTED. If there are not enough bits loaded during ERASE and WRITE instructions prior to CS being brought low, then the operation WILL NOT BE EXECUTED and the Serial EEPROM will return to stand-by.

3 WIRE BUS EXAMPLE

MICROCHIP 93LC66 ERASE CYCLE TIMING DIAGRAM



NOTE: This example is for X8 operation of the MIcrochip's 93LC66. Instruction lengths may vary with array size and data widths.

Data must conform to specified set-up and hold times (Tdis and Tdih) relative to the clock edge. Each parameter is typically 100ns.

AN ERASE operation is identified by a "11 " two bit code that follows the start bit

Next, the address location bits are loaded on the DI pin.

THERE ARE NO DATA BITS TO LOAD. THE ADDRESS LOCATION LOADED WILL BE SET TO AN ERASE STATE OF "1".

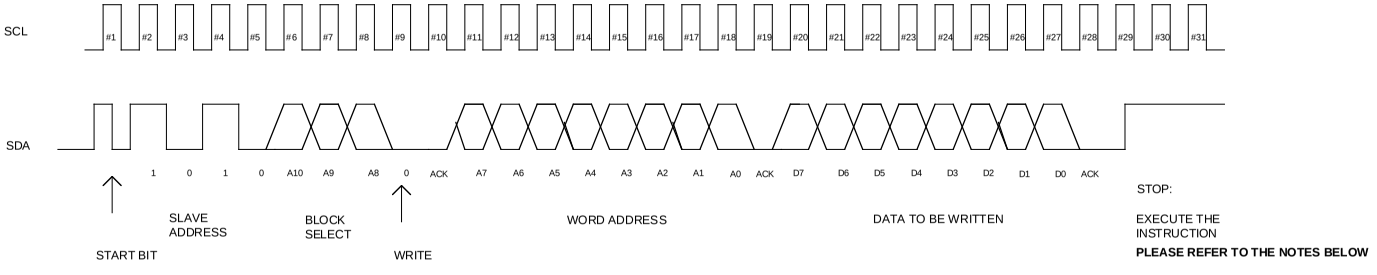
CS must be brought low after the last DI bit is loaded. When CS is brought low for the Tcsl period, a self timed ERASE is executed. If too many bits are loaded during the ERASE and WRITE instructions prior to CS being brought low at the end of an instruction set, then the extra bits will be ignored. Only the first bits loaded will be executed.

The DOUT pin's only function during a ERASE is to indicate the status of the write with the READY/$\overline{\text{BUSY}}$ function. While DOUT islow, the Serial EEPROM is indicating that programming is not complete (the part is BUSY). When Do is high, the Serial EEPROM is indicating that programming is complete and it is READY for another instruction. Note CS must be brought high after completing the Tcsl time is complete to initiate the READY/ $\overline{\text{BUSY}}$ function.

Up through clock pulse 12, the address for the instruction is being LOADED. When CS goes low, the instruction is being EXECUTED.If there are not enough bits loaded during the ERASE and WRITE instructions prior to CS being brought low, then the operation WILL NOT BE EXECUTED and the serial EEPROM will return to stand-by.

2 WIRE BUS EXAMPLE

MICROCHIP 24LC16 BYTE WRITE CYCLE TIMING DIAGRAM



NOTE THE SDA POSITION OF THE START AND STOP BITS. THE SDA TRANSITION IS DURING A HIGH SCL PULSE

ALL OTHER BITS TRANSMITTED MUST COMPLY WITH THE 100KHZ CLOCK IIC PROTOCOL DATA SET -UP TIME (250NS (TSU: DAT) FOR DATA TO BE ESTABLISHED PRIOR TO THE RISING CLOCK EDGE AND THE HOLD TIME O 0NS (THD:DAT) FOR THE FALLING CLOCK EDGE.

THE STOP BIT ON CLOCK PULSE #29 WILL INITIATE A SELF TIMED WRITE. **THE SERIAL EEPROM CAN NOT EXECUTE ADDITIONAL INSTRUCTIONS UNTIL THE CYCLE IS COMPLETE.**

TO EXECUTE A PAGE WRITE, CONTINUE TO LOAD 8 BITS OF DATA AT CYCLE 29 INSTEAD OF ISSUING A STOP BIT (FROM THE MASTER). REMEMBER , A CLOCK PULSE MUST BE ALLOCATED AFTER EACH SUBSEQUENT 8 BITS FOR THE SERIAL EEPROM TO ISSUE AN ACKNOWLEDGE SIGNAL (LOW). AFTER THE DESIRED NUMBER O BYTES HAVE BEEN LOADED, UPTO THEIR PAGE SIZE, THE MASTER MUST ISSUE A STOP BIT TO EXECUTE THE INSTRUCTION.

THE SEQUENCE OF EACH WRITE COMMAND AND THE MASTER/SERIAL DIRECTION OF THE COMMUNICATION IS SHOWN BELOW :

BYTE WRITE

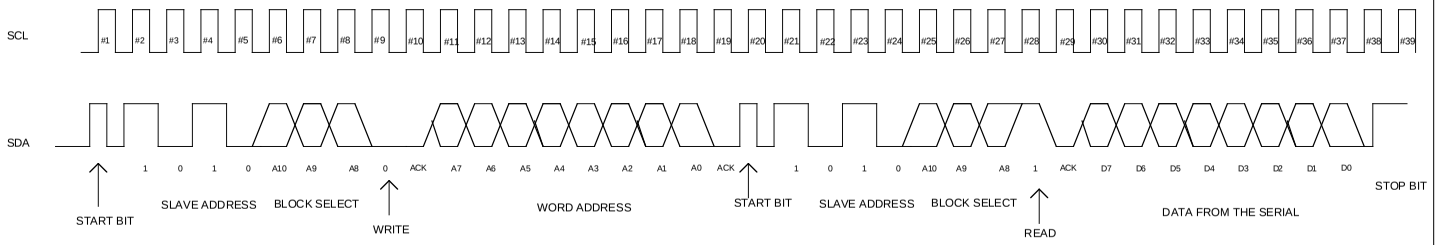
START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
WORD ADDRESS FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
DATA BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
STOP BIT FROM THE MASTER

PAGE WRITE (EXAMPLE WITH 4 BYTES)

START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
WORD ADDRESS FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
DATA BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
DATA BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
DATA BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
DATA BYTE FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
STOP BIT FROM THE MASTER

2 WIRE BUS EXAMPLE

MICROCHIP 24LC16 READ CYCLE TIMING DIAGRAM



NOTE : THE FIRST 19 CLOCK PULSES OF THE WRITE COMMAND ARE IDENTICAL TO THE FIRST 19 CLOCK PULSES IN THE READ COMMAND. EVEN THE 9TH CLOCK PULSE IS A WRITE BIT "0" TO TRANSMIT TO THE SERIAL EEPROM THE DESIRED WORD ADDRESS.

THE READ COMMAND HAS TWO START BITS. THIS IS FOR THE RANDOM READ COMMAND.

AS SHOWN ON THE PREVIOUS PAGES, IF A READ IS DESIRED FROM A CURRENT ADDRESS THEN THE FIRST 19 CLOCK PULSES ARE NOT REQUIRED. THEREFORE, THE FIRST START BIT IS AT CLOCK PULSE #20. THIS IS ONLY FOR THE CURRENT ADDRESS READ COMMAND

ANOTHER USEFUL READ COMMAND IS THE SEQUENTIAL READ COMMAND. THE SEQUENTIAL READ COMMAND IS THE SAME AS THE RANDOM READ COMMAND; HOWEVER, THE MASTER MUST ISSUE AN ACKNOWLEDGE BIT INSTEAD OF THE STOP BIT AS SHOWN FOR CLOCK PULSE #38. THIS SIGNALS THE SERIAL TO READ THE DATA FROM THE NEXT SEQUENTIAL ADDRESS. THE MASTER MUST CONTINUE TO ACKNOWLEDGE EACH BYTE RECEIVED UNTIL THE MASTER ISSUES A STOP BIT.

NOTE THE SDA POSITION OF THE START AND STOP BITS. THE SDA TRANSITION IS DURING A HIGH SCL PULSE

ALL OTHER BITS TRANSMITTED MUST COMPLY WITH THE 100KHZ CLOCK IIC PROTOCOL DATA SET -UP TIME OF 250NS (TSU: DAT) FOR DATA TO BE ESTABLISHED PRIOR TO THE RISING CLOCK EDGE AND THE HOLD TIME OF 0NS (THD:DAT) FOR THE FALLING CLOCK EDGE.

READ (FROM A RANDOM ADDRESS)

START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER (R / W = 0)
ACKNOWLEDGE BIT FROM THE SERIAL
WORD ADDRESS FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER (R / W = 1)
ACKNOWLEDGE BIT FROM THE SERIAL
DATA FROM THE SERIAL
STOP BIT FROM THE MASTER

READ (FROM THE CURRENT ADDRESS)

START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER (R / W = 1)
ACKNOWLEDGE BIT FROM THE SERIAL
DATA FROM THE SERIAL
STOP BIT FROM THE MASTER

READ (Sequential READ of 3 bytes)

START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER (R / W = 0)
ACKNOWLEDGE BIT FROM THE SERIAL
WORD ADDRESS FROM THE MASTER
ACKNOWLEDGE BIT FROM THE SERIAL
START BIT FROM THE MASTER
CONTROL BYTE FROM THE MASTER (R / W = 1)
ACKNOWLEDGE BIT FROM THE SERIAL
DATA FROM THE SERIAL
ACKNOWLEDGE BIT FROM THE MASTER
DATA FROM THE SERIAL
ACKNOWLEDGE BIT FROM THE MASTER
DATA FROM THE SERIAL
STOP BIT FROM THE MASTER

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