ispGDX™ and ispGDS™ Architectural Description

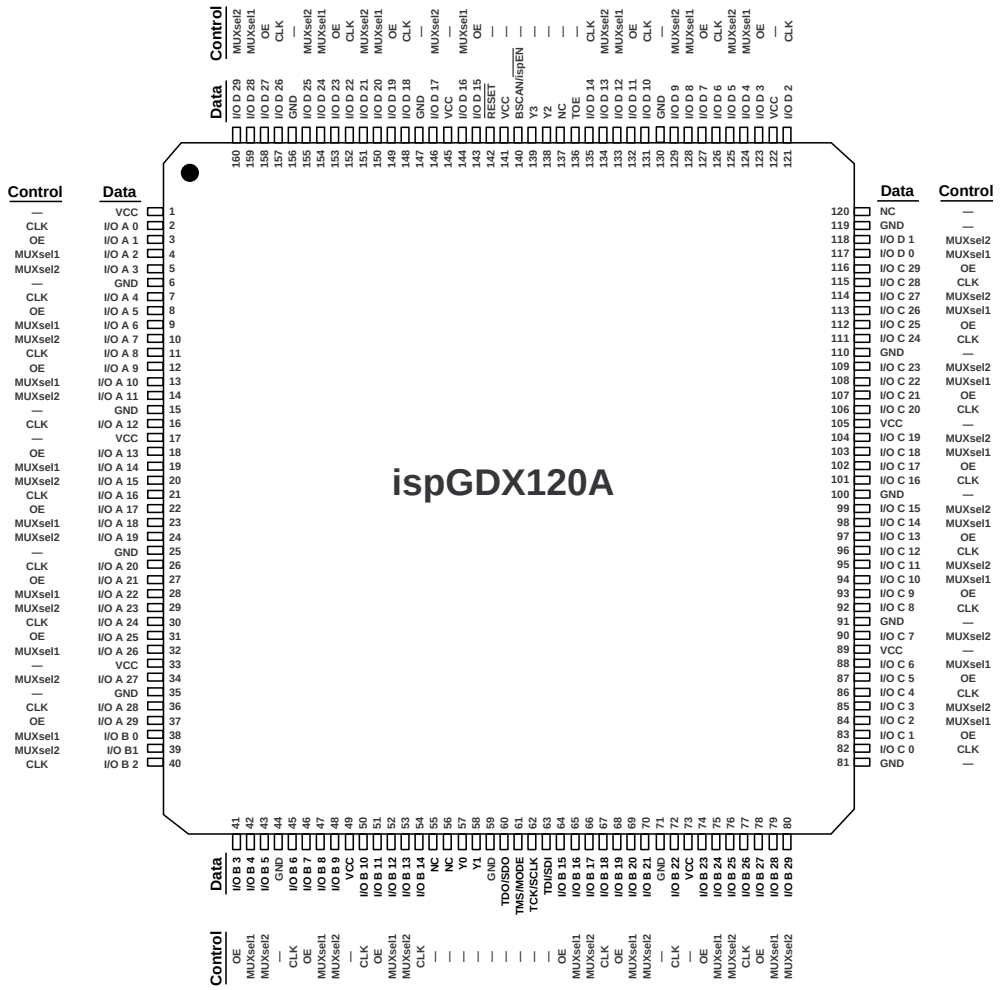
ispGDX Family

The architecture of the ispGDX family of devices consists of a series of programmable I/O cells interconnected by a Global Routing Pool (GRP). The GRP is a proprietary interconnect structure from Lattice Semiconductor, pioneered in the ispLSI family, that allows any input to be connected to any one or more outputs on the device. Unlike ispLSI devices, there are no programmable logic arrays on ispGDX devices. Control signals for OE's, Clocks and MUX Controls must come from designated sets of I/O pins.

Each I/O cell drives a unique pin. The I/O cells include a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. Each I/O cell has individual, programmable tri-state control (OE), register or latch clock, (CLK), and programmable polarity. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O-OE pins. Using the individual tri-state control it is possible to emulate open-drain output functionality for wired-OR bus applications.

Each I/O cell also contains a 4:1 dynamic MUX controlled by two select lines called MUX0 and MUX1. The four data inputs to the MUX (called MUXA, MUXB, MUXC, and MUXD) come from I/O signals found in the GRP. Each MUX data input can be accessed by one quarter of the total I/Os. MUX0 and MUX1 can be driven by designated I/O pins called the MUXsel pins. MUXsel inputs can be chosen from designated pins — see Figure 1.

Figure 1. ispGDX120A Pinout



As shown in Figure 2, when both register/latch control muxes select the “A” path, the register/latch gets its inputs from the 4:1 mux and drives the I/O output. When selecting the “B” path the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O clock set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Yx). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass mux. I/O cell polarity can be programmed as active high or active low. Finally, outputs may be set to fixed HIGH or LOW logic levels to simulate Jumper or DIP Switch functions.

Device output buffers have balanced 24mA drive as well as independently programmable output slew rate to reduce overall ground bounce and switching noise. IEEE1149.1-compliant Boundary Scan test is supported by dedicated registers at each I/O pin (see Figure 3).

In-system programming is supported through the Test Access Port via a special set of private commands (Boundary Scan protocol) or through the Lattice ISP protocol. The programming protocol is selected by the BSCAN/$\overline{\text{ispEN}}$ pin.

ispGDS Family

The ispGDS architecture features a programmable switch matrix surrounded by two banks of programmable I/O macrocells. The I/O cells in each device are divided equally into two banks (Bank A and Bank B). Each I/O macrocell can be configured as an input, an inverting or non-inverting output or a fixed TTL HIGH or LOW output. The switch matrix connects the I/O banks, allowing an I/O cell in one bank to be connected to any of the I/O cells in the other bank. A single I/O cell configured as an input can drive one or more I/O cells in the other bank.

Figure 2. ispGDX I/O Cell and GRP Detail (160 I/O Device)

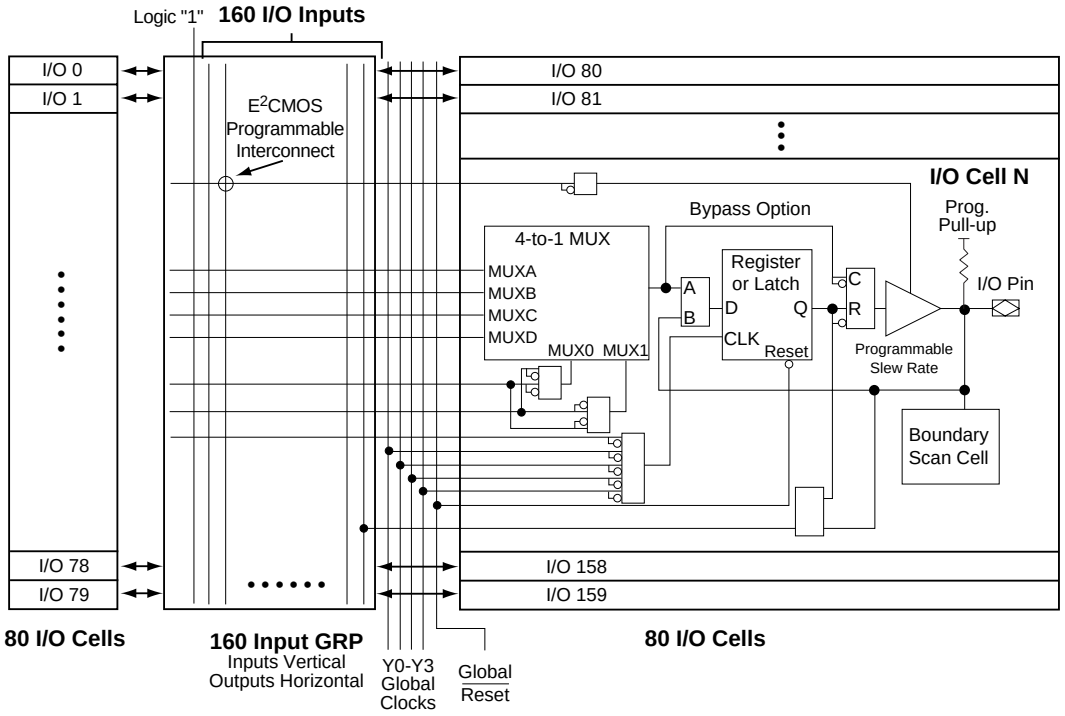


Figure 3. ispGDX Boundary Scan I/O Register Cell

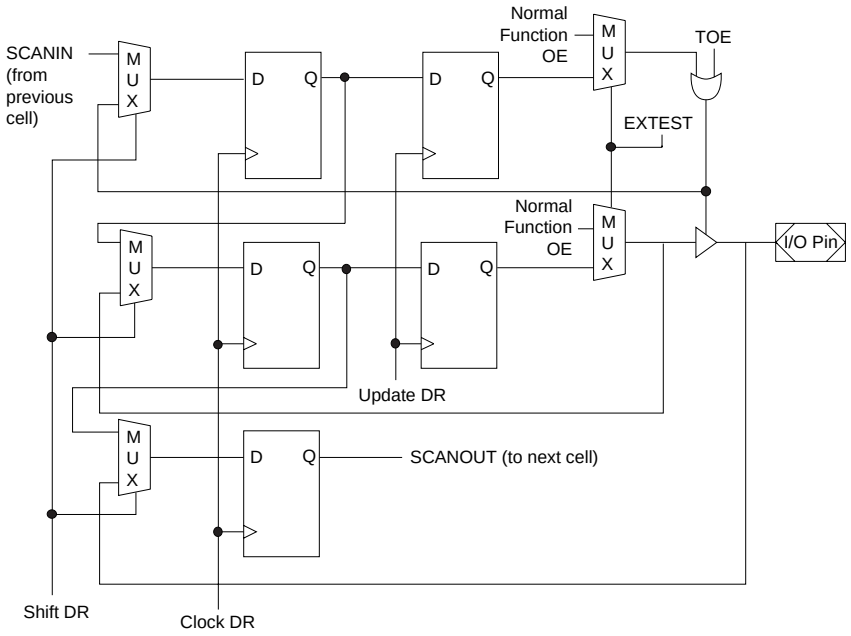


Figure 4. ispGDS22 Functional Block Diagram